OIPE JC130
APR 1 2 2004
PATENT & TRADEMARK OFFICE

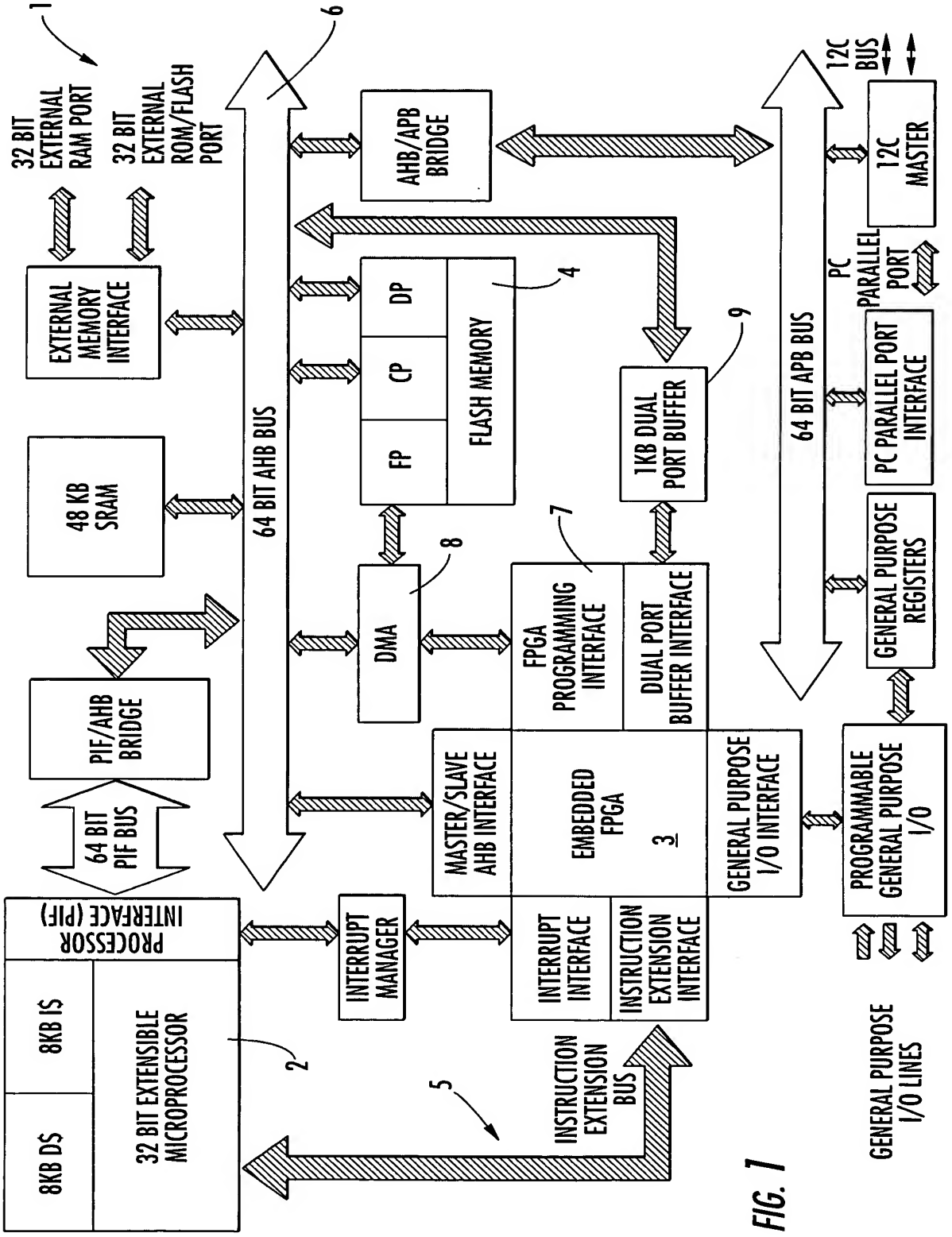


FIG. 1

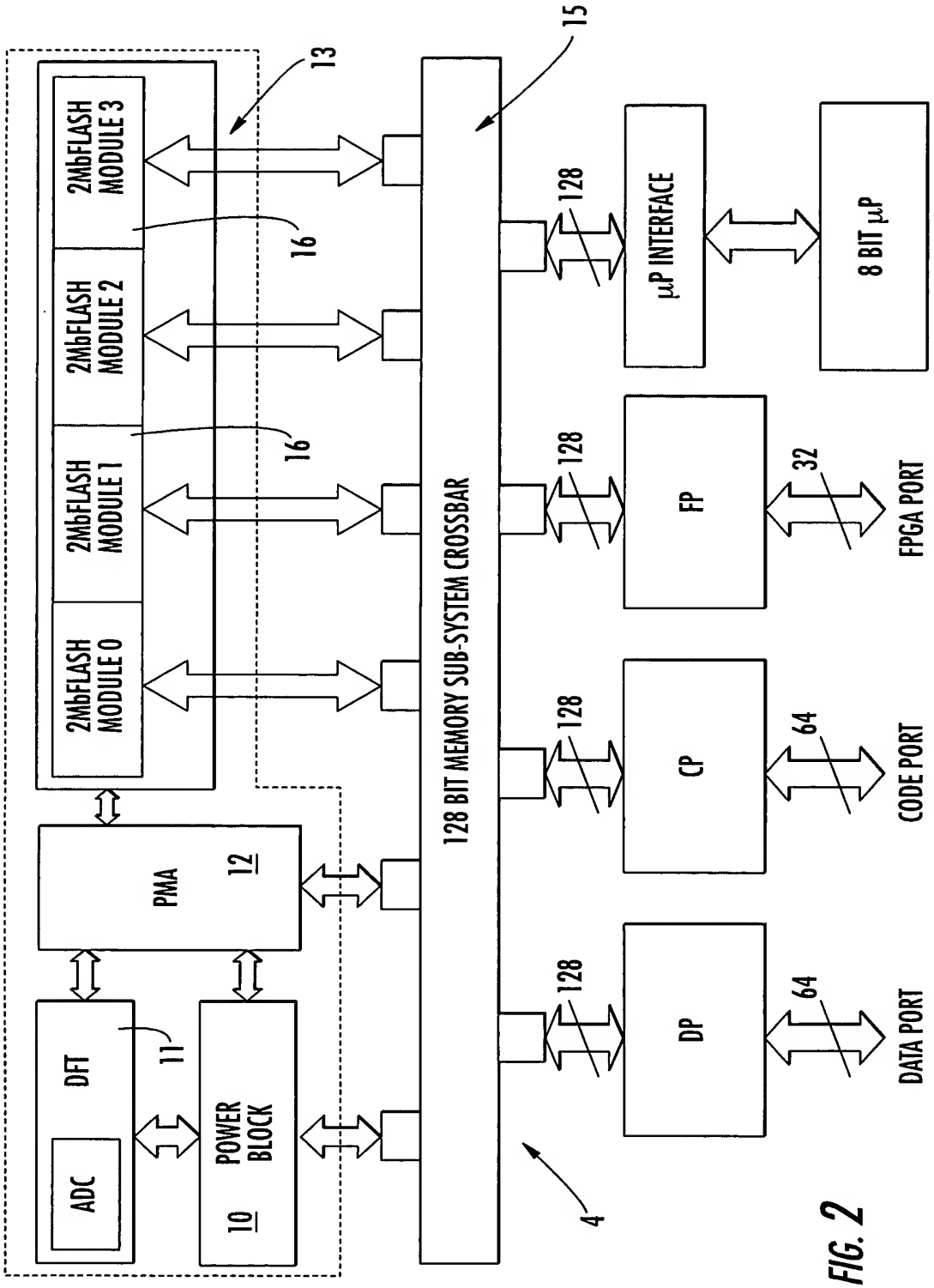

2MbFLASH MODULE 3
2MbFLASH MODULE 2
2MbFLASH MODULE 1
2MbFLASH MODULE 0
13
15
16
16
PMA
12
DFT
11
ADC
POWER BLOCK
10
128 BIT MEMORY SUB-SYSTEM CROSSBAR
4
128
µP INTERFACE
8 BIT µP
128
FP
32
FPGA PORT
128
CP
64
CODE PORT
128
DP
64
DATA PORT

FIG. 2

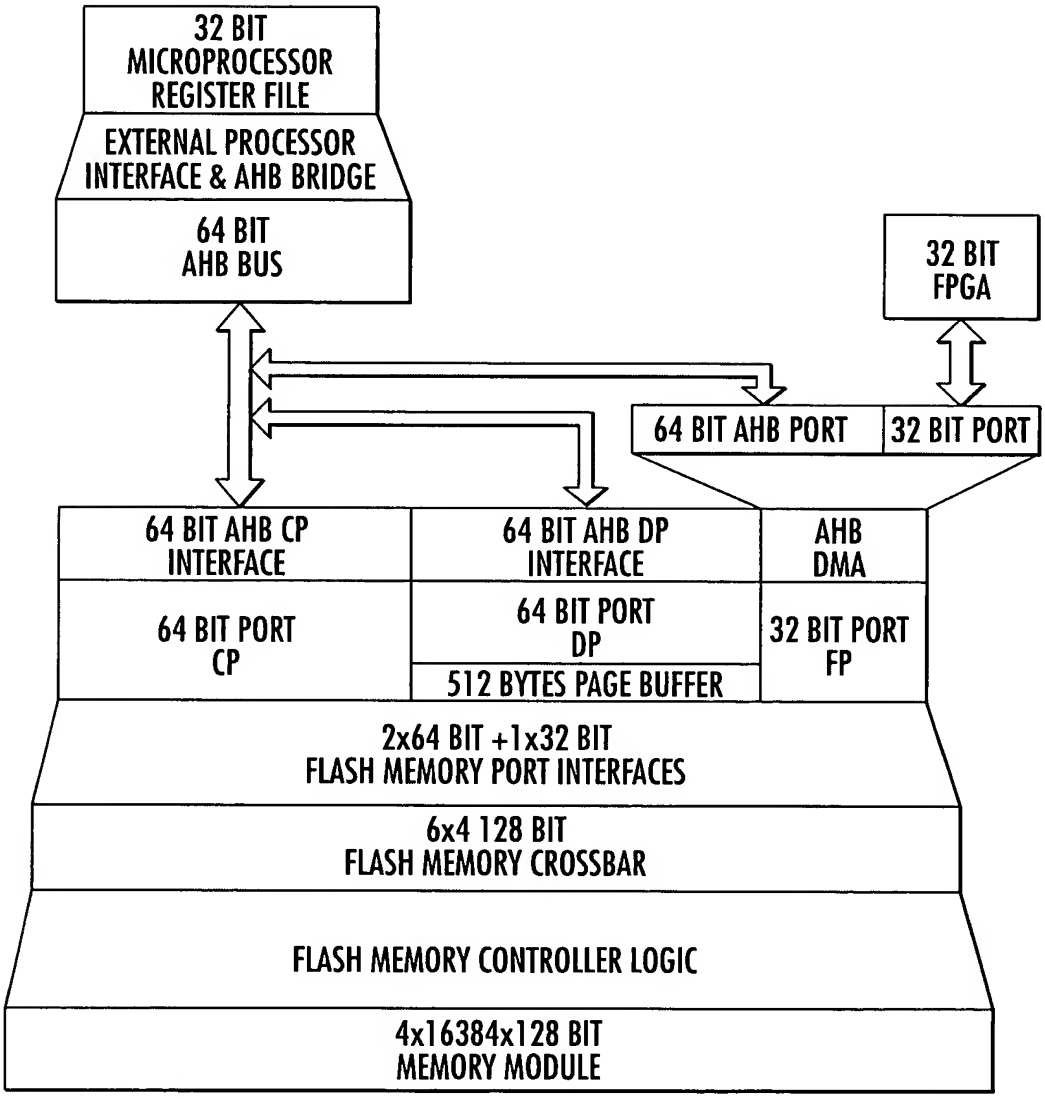
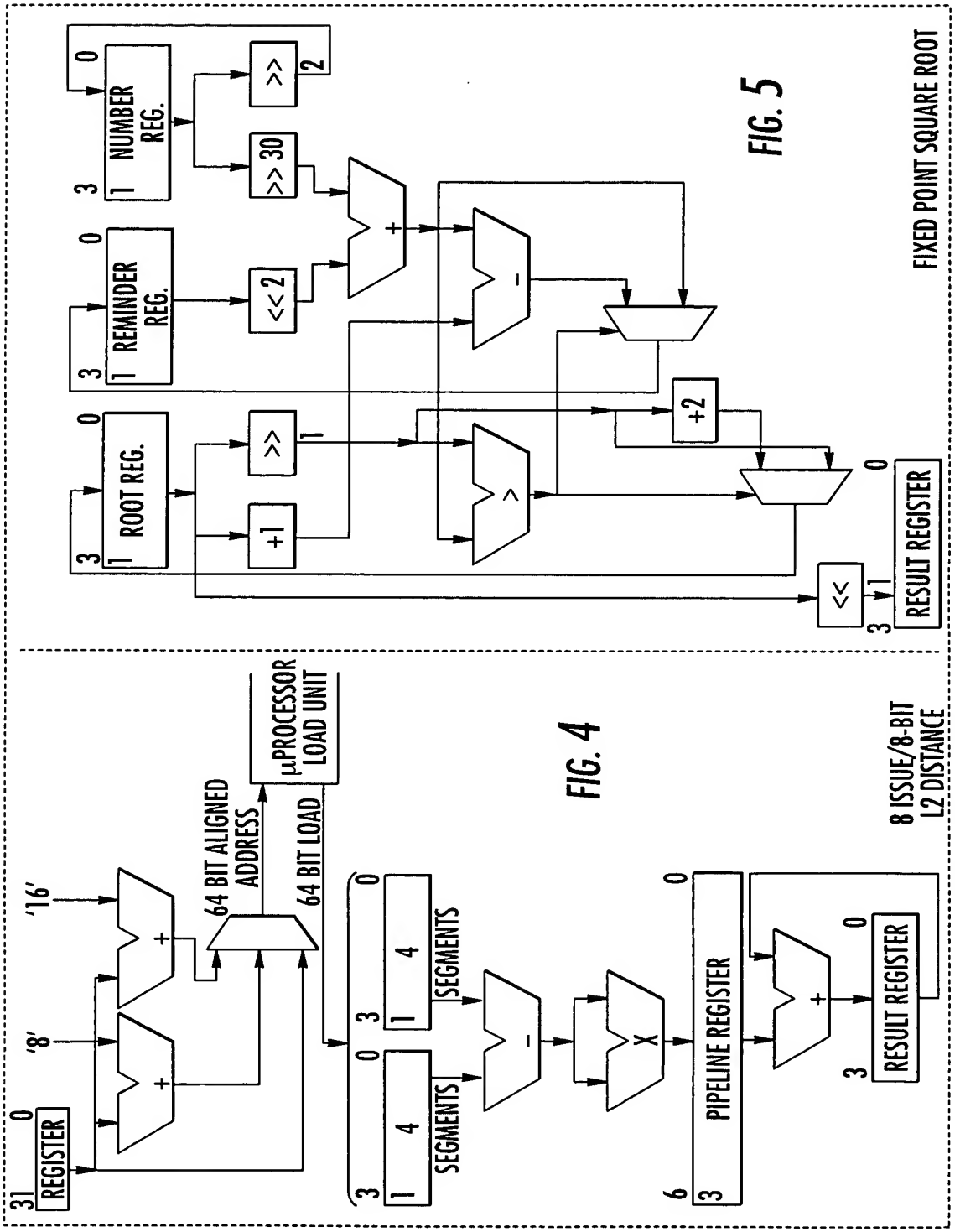

32 BIT
MICROPROCESSOR
REGISTER FILE
EXTERNAL PROCESSOR
INTERFACE & AHB BRIDGE
64 BIT
AHB BUS
32 BIT
FPGA
64 BIT AHB PORT
32 BIT PORT
64 BIT AHB CP
INTERFACE
64 BIT AHB DP
INTERFACE
AHB
DMA
64 BIT PORT
CP
64 BIT PORT
DP
512 BYTES PAGE BUFFER
32 BIT PORT
FP
2x64 BIT +1x32 BIT
FLASH MEMORY PORT INTERFACES
6x4 128 BIT
FLASH MEMORY CROSSBAR
FLASH MEMORY CONTROLLER LOGIC
4x16384x128 BIT
MEMORY MODULE

FIG. 3


FIXED POINT SQUARE ROOT
ROOT REG.
REMINDER REG.
NUMBER REG.
RESULT REGISTER
+1
+2
>>
<<2
>> 30
>> 2
<<
FIG. 5
8 ISSUE/8-BIT L2 DISTANCE
REGISTER
'16'
'8'
64 BIT ALIGNED ADDRESS
64 BIT LOAD
µPROCESSOR LOAD UNIT
SEGMENTS
SEGMENTS
PIPELINE REGISTER
RESULT REGISTER
FIG. 4

ALGORITHM STAGE	RISC WITH BASIC DSP INSTRUCTION SUPPORT	RISC WITH MICROPROCESSOR EXTENSIONS	SPEED UP	ENERGY GAIN	ENERGY EFFICIENCY GAIN (ENERGY x DELAY)
BAYER FILTER	58 MSEC	24.7 MSEC	x2.3	x1.4	x3.22
EDGE DETECTION	4.5 MSEC	2.5 MSEC	x1.8	x0.95	x1.71
FACE DETECTION	1.5 SEC	382 MSEC	x4	x2.9	x11.6
FACE RECOGNITION (TWENTY FACE DATABASE)	9.15 SEC	860 MSEC	x10.6	x9	x95.4
TOTALS	10.7 SEC	1.26 SEC	x8.5	x6.7	

FIG. 6

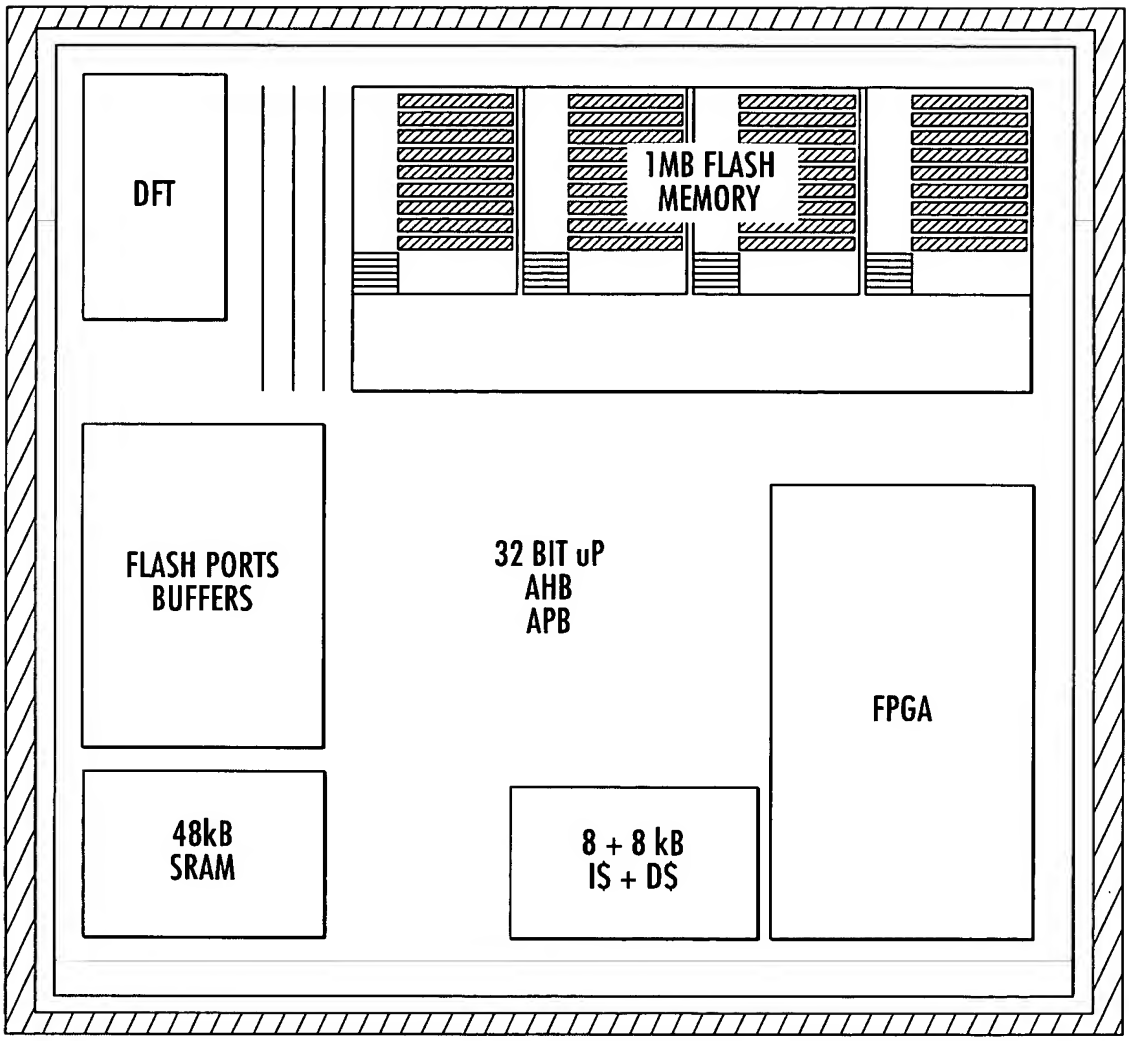

DFT
1MB FLASH
MEMORY
FLASH PORTS
BUFFERS
32 BIT uP
AHB
APB
FPGA
48kB
SRAM
8 + 8 kB
I$ + D$

FIG. 7